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(54) Controlling a power state of a computer

(57) Method and apparatus of controlling a power state of a computer, the computer being connected to a monitor having a power control button. The computer is connected to the monitor over a video cable, and activation of the power control button is communicated to the computer over a wire in the video cable. In response to the activation signal, a system management interrupt is generated to invoke an SMI handler to change the power state of the computer. The power states of the computer include an ON state, an intermediate power state (such as Sleep state), and a suspend state (such as Soft-Off state).

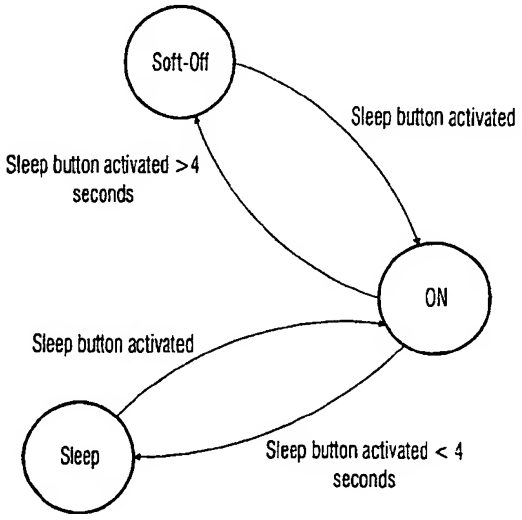

Figure 1

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Description

The invention relates to controlling a power state of a computer.

The main power switch, located on a computer's housing, has typically been used to power the computer on and off. In a continuing effort to make it more convenient for a user to control the power state of a computer, other ways of powering down the computer have been developed. For example, the Advanced Power Management (APM) (Version 1.2) standard has defined a Soft-Off state that software in the computer can transition to. Operating systems (such as Windows® from Microsoft Corporation) that support the APM Soft-Off state allow a user to place the computer into the Soft-Off state directly from the graphical user interface of the operating system (such as from the Start menu in the Windows 95® user interface).

An example of a hardware device that can interface with the Windows® operating system to place the computer into Soft-Off state is the 82371AB PCI-TO-ISA/IDE XCELERATOR (PIIX4) sold by Intel Corporation, which includes a system power management controller to manage transitions of the computer power state, including the Soft-Off state.

The invention may have one or more of the following advantages. By using a power switch located on a computer's monitor to control a power state of the computer, a user is provided a more convenient means of switching the state of the computer. The power control is accomplished using the existing wires of the video cable connecting the computer and monitor, thereby avoiding adding signal lines between the computer and the monitor.

Other advantages and features will become apparent from the following description and the claims.

In general, in one aspect, the invention features a method of controlling a power state of a computer, the computer being connected to a monitor having a power control button. Activation of the monitor power control button is received, and the power state of the computer is changed in response to activation of the monitor power control button.

Implementations of the invention may include one or more of the following features. The computer is connected to the monitor over a video cable, and an activation signal representing activation of the monitor power control button is received over a wire of the video cable. The video cable includes a VGA cable. The VGA cable includes a pin 4, and the activation signal is transmitted through pin 4. The power control button includes a Sleep button, and the computer includes the following power states: ON state, intermediate power state, and suspend state. The intermediate power state includes a Sleep state, and the suspend state includes a Soft-Off state.

In general, in another aspect, the invention features a method of controlling a power state of a computer, the computer being connected by a VGA cable to a monitor having a power control button. An activation signal is received over a wire in the VGA cable in response to activation of the monitor power control button. A system management interrupt is generated in response to receipt of the activation signal. A system management interrupt handler is invoked to change the power state of the computer. The computer includes an ON state, an intermediate power state, and a suspend state.

In general, in another aspect, the invention features a computer system including a monitor having a power button and a power management controller coupled to the monitor. The power management controller is configured to change the power state of the computer system in response to activation of the monitor power button.

In general, in another aspect, the invention features a computer system having a power control switch and a power management controller. The power management controller is connected to receive activation of the power control switch, the power management controller capable of placing the computer system into one of a Sleep state and a Suspend state.

Fig. 1 is a state diagram illustrating the different states of a computer.

Fig. 2 is a block diagram of a computer connected to a display monitor.

Fig. 3 is a front view of a video graphics adaptor connector.

Fig. 4 is a schematic diagram of power control circuitry in the computer.

Fig. 5 is a flow diagram of firmware for controlling a microcontroller in the display monitor.

Fig. 6 is a flow diagram of a BIOS routine to enable the power control feature of the computer.

Fig. 7 is a flow diagram of a system management handler for transitioning the computer to the proper power state.

A computer has several power states, including an ON state, an intermediate power state, a suspend state, and a hard OFF state. One example of an intermediate power state is the Sleep state, in which various system clocks are shut down to conserve power. In the suspend state (such as the Soft-Off state), many of the computer's power supply voltages are disabled. In the hard OFF state, all power supply voltages are disabled.

The power state of the computer is controlled using a Sleep button on a computer's monitor connected to the computer by a video cable, e.g., a video graphics adaptor (VGA) cable. To avoid adding wires between the computer and monitor, an existing wire in the VGA cable is used to communicate an activation signal representing the state of the monitor's Sleep button.

Alternatively, activation of the SLEEP signal can be transmitted over a serial bus connecting the monitor and computer. The activation signal is transmitted to a power management controller located in the computer to switch the computer into one of three power states: ON,

intermediate (e.g., Sleep), and suspend (e.g., Soft-Off).

The following description discusses circuitry and steps of programs to transition the computer between the Soft-Off and Sleep states. Similar circuitry and steps can be used to transition the computer between other suspend and intermediate power states.

Referring to Fig. 1, if the computer is in either of the Soft-Off or Sleep states, activation of the Sleep button on the monitor causes the power management controller to transition the computer to the ON state. Once in the ON state, the computer can transition back to either the Sleep state or the Soft-Off state, depending on how long the user activates the Sleep button. If the Sleep button is activated less than a predetermined time period (e.g., 4 seconds), the power management controller causes the computer to transition to the Sleep state; otherwise, if the Sleep button is pressed for greater than or equal to the predetermined time period, the power management controller causes the computer to transition to the Soft-Off state.

Software, such as a system management interrupt (SMI) handler, is used to transition the computer out of either the ON or Sleep states, as the computer is powered on in these states and all necessary software, including device drivers, remain available. A hardware reset (to reboot the computer) is used to transition the computer out of the Soft-Off state, as most of the components of the computer are powered down in this state.

Referring to Fig. 2, a computer 8 is connected to a monitor 6 by a Universal Serial Bus (USB) cable 12 and a video cable 14 (such as a video graphics adaptor or VGA cable) through two connectors 110 and 112, respectively. Video signals are communicated between the computer 8 and the monitor 6 over the VGA cable 14. The USB cable 12 can be used to communicate other types of information (e.g., configuration data and control data) between the monitor 6 and the computer 8.

The monitor 6 has two power management buttons: a main power button 114 connected to the monitor's power supply 116; and a Sleep button 118 connected to provide a SLEEP signal to a microcontroller 104. Pressing the power button 114 shuts down the power supply 116, thereby cutting off power to all components in the monitor 6. The Sleep button 118 can be activated by the user to transition the computer 8 to one of several states: ON, Sleep, and Soft-Off.

The microcontroller 104, running under control of firmware, can transmit activation of the Sleep button over either the USB cable 12 or the VGA cable 14, or both, depending upon the states of power control bits in a microcontroller configuration register 120.

In the computer 8, all video signals, except for one, in the VGA cable 14 are routed through the connector 112 to a video controller 108 in the computer 8. The video signals include the HSYNC and VSYNC synchronization signals provided to the monitor by the video controller 108. When the computer 8 is placed into either the intermediate power state (e.g., Sleep) or the suspend state (e.g., Soft-Off), the HSYNC and VSYNC signals are disabled by the video controller 108 to blank the monitor screen.

The remaining signal (designated VOLUP_) in the VGA cable 14 is routed to an inverter 122, which drives a signal LID to a PCI-ISA bridge 124 (such as the 82371AB PCI-TO-ISA/IDE XCELERATOR or PIIX4 chip from Intel Corporation). The LID input is provided to a system power management controller 126 in the PCI-ISA bridge 124. The system power management controller 126 performs various power management functions in the computer 8, as discussed in greater detail below.

Separately, the USB signals in the USB cable 12 are routed through the connector 110 to a USB interface controller 128 in the PCI-ISA bridge 124. The USB cable 12 includes a serial line 182 and a power line 180. The serial line 182 is used to communicate control and data bits. The power line 180 is activated to a high voltage state (e.g., 5 volts) when the computer 8 is on or in Sleep mode. The power line 180 is low if the computer 8 is in Soft-Off mode.

The PCI-ISA bridge 124 controls communications between a Peripheral Component Interconnect (PCI) bus 106 and an Industry Standard Architecture (ISA) bus 132. Also connected to the PCI bus 106 are the video controller 108, a SCSI controller 134, and a CPU-PCI bridge 104. The CPU-PCI bridge 104 is connected on its other side to a CPU (central processing unit) 100 and to a main memory 102. The SCSI controller 124 is connected to a hard disk drive 136.

In addition, an input/output (I/O) controller 140, a non-volatile random access memory (NVRAM) 142, and ISA slots 144 are connected to the ISA bus 132. The I/O controller 140 provides interface ports to a floppy disk drive 146, a keyboard 148, and a pointer device 150. The I/O controller also includes a control circuit for the NVRAM 142, which can be implemented with an electrical erasable programmable read-only memory (EEPROM) or flash memory. Basic input/output system (BIOS) routines are stored in the NVRAM 142, which are invoked during the power-up sequence of the computer as well as in response to power management calls made by the operating system running on the computer 8.

A power supply 152 provides various supply voltages to other components in the computer 8, including supply voltages VCC(CORE), VCC(RTC), VCC(SUS), and VCC(USB) connected to the PCI-ISA bridge 124. The different VCC signals power various parts of the PCI-ISA bridge 124, with the VCC(CORE) voltage supplied to the majority of the components in the PCI-ISA bridge 124, the VCC(RTC) voltage applied to the real time clock, the VCC(SUS) voltage supplied to the system power management controller 126, and the voltage VCC(USB) supplied to the USB interface controller 128.

Alternatively, the voltages VCC(USB) and VCC (CORE) can be the same voltage.

The power supply 152 generates a signal PWROK

to indicate when the power supply voltages in the computer 8 have stabilized at their predefined levels, e g. about 3.3 volts for VCC(CORE), VCC(RTC), VCC (SUS), and VCC(USB). The system power management controller 126 in the PCI-ISA bridge 124 provides a suspend signal SUSC_ to an inverter 154, which in turn drives a signal SUSC to the power supply 152. The inverter 154 is all connected to the supply voltage VCC (SUS). The SUSC signal is activated to place the computer 8 into the Soft-Off mode and cause the power supply 152 to disable all power voltages except for VCC (RTC) and VCC(SUS) to the PCI-ISA bridge 124. When the computer is off, the voltage VCC(RTC) is actually sourced by a lithium battery.

The system power management controller 126 also receives a signal POWERBTN_ from a Bezel power button 156 located on the housing of the computer 8 In response to activation of the POWERBTN_ signal, the system power management controller 126 can place the computer 8 to either the Sleep state or the Soft-Off state.

A separate, main power button 158 located on another part of the computer housing switches the computer completely on or off. When switched off, the power supply 152 disables all voltage signals in the computer 8 except VCC(RTC) for the real time clock.

A further means for the user to control the power state of the computer is through the graphical user interface of the operating system (e.g., Windows 95®). In the Windows 95® interface, the user can select the Start menu to shut down the computer. If the user specifies the shut-down command, the computer 8 invokes various routines to cause the system power management controller 126 and the PCI-ISA bridge 124 to activate the suspend signal SUSC_ to disable various voltages generated by the power supply 152.

Use of the Sleep button 118 on the monitor 6 to control the power state of the computer 8 is described below in greater detail. The state of the Sleep button 118 is transmitted either over the VGA cable 14 or the USB cable 12 by the microcontroller 104 depending upon the states of the power control bits in the configuration register 120 in the microcontroller 104. The contents of the configuration register 120 can be set over the USB cable 12 by software running on the computer 8. The software controls the USB interface controller 128 in the PCI-ISA bridge 124 to perform a sequence of cycles on the USB bus 12 to write the appropriate bits into the configuration register 120.

Referring to Fig. 5, the microcontroller 104 in the monitor 6 is run under control of firmware, which determines whether the signal SLEEP is routed over the USB cable 12 or the VGA cable 14. The firmware checks at step 302 whether the signal SLEEP is asserted. What the firmware does next depends upon the state of the computer 8. If the firmware determines at step 306 that the computer 8 is in Sleep state, then it performs one of steps 316, 318, 320, or 322. Before the computer 8 enters into Sleep mode, the USB interface controller 128 in the PCI-ISA bridge 124 sends a sleep notification over the USB cable 12, which is stored by the microcontroller 104 as a sleep bit in an internal register (not shown). If the stored sleep bit is active and the USB power line 180 is active (at 5 volts), then the computer 8 is determined to be in Sleep mode.

The firmware determines at steps 308, 310, 312 and 314 whether the SLEEP signal is to be transmitted over the USB cable 12, VGA cable 12, both cables, or neither cable. If over the USB cable, a USB resume command is transmitted. If over the VGA cable 14, the SLEEP signal is routed over wire 4 of the VGA cable (as shown in Fig. 3) and passed through the VGA connector 112 as the signal VOLUP_. If the sleep indication is to be sent over both cables 12 and 14, then activation of the SLEEP signal is sent over the USB cable and wire 4 in the VGA cable is activated. If the sleep indication is to be sent over neither cable, then no action is taken.

If the computer 8 is determined to be in the ON state (the stored sleep bit is low and the USB power line 180 is active), then one of the steps 334, 336, 338, and 340 is performed, depending on whether the sleep indication is to be transmitted over the USB cable, the VGA cable, both cables, or neither cable, as determined at steps 326, 328, 330, and 332. A sleep command is sent over the USB cable 12, and/or the SLEEP signal is activated over wire 4 of the VGA cable.

Finally, if the computer 8 is determined to be in the Soft-Off mode (the USB power line 180 is inactive), then one of steps 352, 354, 356, and 358 is performed, depending on which cables are to be used for notification as determined at steps 344, 346, 348, and 350. A resume command is sent over the USB cable, and the SLEEP signal is activated over wire 4 of the VGA cable.

If the PIIX4 controller is used, however, transmission of the resume command over the USB cable is ignored if the computer is in the Soft-Off mode, since the USB interface controller 128 is powered down. To take advantage of the ability to route activation of the SLEEP signal over the USB bus, the voltage VCC(USB) would be maintained to the USB interface controller 128, which would decode a resume or sleep command received over the USB bus from the monitor 6 and respond by invoking power management routines to control the state of the computer 8.

Described below is the implementation in which the activation of the SLEEP signal is routed over the VGA cable. However, the described implementation can be easily modified and extended to communication of the SLEEP signal over the USB bus.

Referring to Fig. 4, in the computer 8, the signal VOLUP_ from the VGA cable 14 is routed to the inverter 122, which includes an NPN transistor 206 having its base connected through a resistor 204 to receive the signal VOLUP_ and its emitter connected to ground. The collector of the transistor 206 is connected through a resistor 208 to the power supply voltage VCC(SUS), which is not disabled during Soft-Off mode. A resistor

202 is further connected between VCC(SUS) and the signal VOLUP_. In addition to acting as an inverting buffer for the signal VOLUP_ from the VGA cable 14, the circuitry of the inverter 122 also provides overvoltage protection in case the monitor 6 connected to the computer 8 is a monitor that does not support routing the SLEEP signal over the VGA cable.

The inverter 122 outputs the signal LID, which is provided to the LID_ input of the PCI-ISA bridge 124. As the signal LID is a non-inverted signal (i.e., active high), the LID polarity bit (LID_POL) in a configuration register in the PCI-ISA bridge 124 is set to indicate a non-inverting polarity at the LID_ input. This is further described in Intel Corporation, 82371AB PCI-TO-ISA/IDE XCELERATOR (PIIX4) Specification (April 1997), which is hereby incorporated by reference in its entirety.

For purposes of identifying the type of monitor connected to the computer 8, digital data channel (DDC) lines 210 in the VGA cable 14 connected to the video controller 108 are used. The DDC lines 210 are connected to a monitor-type configuration register (not shown) in the monitor 6 that stores a value indicating the type of monitor. During the power-up sequence, the system BIOS routine checks the value of this configuration register over the DDC lines 210 to determine if the monitor supports routing the SLEEP signal over the VGA cable 14 (referred to as a "power control-type monitor").

Referring to Fig. 6, a system BIOS routine is invoked during POST (power on self-test) in the computer boot process. At step 402, the BIOS routine performs initial POST functions. Next, at step 404, the BIOS routine initializes SMI handlers by copying them from the NVRAM 142 to SMRAM, located in the main memory 102.

Next, at step 406, the BIOS routine determines if the user has explicitly enabled a power control-type monitor in CMOS setup. The user can enter the CMOS setup screen by hitting a predefined key (e.g., F10 key) during POST, which allows the user to select one of three options with respect to a power control-type monitor field: ENABLE, DISABLE, or AUTODETECT. If the user specifies ENABLE, then the computer 8 treats the monitor 6 as a power control-type monitor. If the user specifies DISABLE, then the computer 8 treats the monitor 6 as a non-power control-type monitor. If the user specifies AUTODETECT, then the computer 8 performs automatic detection to determine the type of monitor over the DDC lines 210.

Thus, at step 406, if the CMOS set-up has enabled the power control-type monitor, then the BIOS routine proceeds to enable at step 408 the LID pin in the PCI-ISA bridge 124. The BIOS routine performs this by setting a lid enable (LID_EN) bit high in a general purpose enable register in the PCI-ISA bridge 124. A more detailed description of the configuration register set in the PIIX4 chip is described in the 82371AB PCI-TO-ISA/IDE XCELERATOR (PIIX4) Specification, referenced above. The BIOS routine then finishes the remaining POST functions at step 414.

If the CMOS setup specifies AUTODETECT, then the BIOS routine automatically determines at step 410 if the monitor connected to the computer 8 is a power control-type monitor. As explained above, this is performed by accessing the monitor-type configuration register in the monitor 6 over the DDC lines 210. If the BIOS routine determines that a power control-type monitor is attached, it enables at step 408 the LID pin in the PCI-ISA bridge 124.

If a power control-type monitor is not connected (either disabled in CMOS set-up or after a determination over the DDC lines 210), the BIOS routine at step 412 determines if a volume control-type monitor is attached. As described in U.S. Application Serial No. 08/667,582, filed July 12, 1996, entitled "Controlling Multi-Media Aspects of a Computer" and having the same assignee as the present application, a computer monitor has a volume control knob on its housing connected to a volume control circuit (not shown) in the monitor. The co-pending application is hereby incorporated by reference. As explained in the application, the monitor volume control circuit is responsive to movement of the volume control knob and communicates decoded signals VOLUP_ and VOLDOWN_ (not shown) over the VGA cable 14, such as through pins 4 and 11 (Fig. 3). The signals are provided to a sound chip 170 connected to the ISA bus 132 to control the volume of sound emanating from speakers connected to the computer 8.

The volume control capability of the sound chip 170 is enabled by a signal VOL_EN_, which is set active (low) by the I/O controller 140 in response to enabling by the BIOS routine after the BIOS routine determines that a volume control-type monitor is attached to the computer 8 (at step 412). If a power-control type monitor or a standard monitor is attached to the computer 8, then the signal VOL_EN_ is deasserted (high) to disable the volume control feature.

If the lid enable (LID_EN) bit in the general purpose enable register of the PCI-ISA bridge 124 is set high, and the signal LID is asserted high by the inverter 122 (subject to up to a 4-ms debouncing by the system management controller 126), the system management controller 126 asserts the system management interrupt SMI_ to the CPU 100. This causes the CPU 100 to invoke an SMI handler.

Referring to Fig. 7, the SMI handler determines at step 502 the type of SMI that has been invoked. Whether the type of SMI handler is an LID SMI is indicated by an LID status bit (LID_STS) set high in the general purpose status register of the PCI-ISA bridge 124. If the event is not an LID SMI as determined by step 504, the SMI handler performs steps to service the other type of SMI at step 506 and exits.

If the event is an LID SMI, the SMI handler checks at step 508 whether a parameter TSLEEP is greater than 4, which represents that the user has pressed the Sleep button 118 on the monitor 6 for greater than or

equal to 4 seconds. The user can place the computer 8 into either the Sleep state or the Soft-Off state, depending on how long the user presses the Sleep button 118 on the monitor 6. If the Sleep button 118 is pressed for less than the predetermined time period (e.g., 4 seconds) and released, the computer 8 is placed into the Sleep state; otherwise, if the Sleep button 118 is pressed for more than or equal to the 4 seconds (the "4-sec override"), the computer 8 is placed into the Soft-Off state. The parameter TSLEEP is initialized to the value one.

To time the Sleep button 118, the SMI handler works with a one-second timer routine To avoid staying in SMI for 4 seconds, which is undesirable since all other interrupts in the computer 8 are masked during an SMI event, the SMI handler exits after it invokes this one-second timer routine to count the one-second time period. After the one-second timer routine finishes counting one second, it reinvokes the LID SMI handler.

This process is shown by steps 508, 512, and 514 of the SMI handler in Fig. 7. If the parameter TSLEEP is not greater than or equal to 4 (TSLEEP is initialized to 1), then 4 seconds have not elapsed during which the user is continuously pressing the Sleep button 118, then the SMI handler checks at step 512 if the LID signal has been deasserted by checking the LID status bit (LID_STS) in the general purpose status register of the PCI-ISA bridge 124. If the LID signal remains asserted (indicating that the Sleep button 118 is still being pressed by the user), the SMI handler at step 514 increments the parameter TSLEEP, restarts the one-second timer routine, and exits.

If, however, the LID signal is deasserted at step 512, the SMI handler can proceed to transition the computer into or out of Sleep state. At step 510, the SMI handler determines if it is currently in the ON state. If so, the SMI handler proceeds at step 516 to transition the computer 8 to Sleep state. In transitioning to the Sleep state, the SMI handler issues a call to the video controller 108 to shut off the HSYNC and VSYNC clocks to blank the monitor 6. However, if the computer is not currently in the ON state, that indicates that the computer 8 is in the Sleep state and the SMI handler proceeds to step 518 to transition the computer 8 back to the ON state.

The 4-sec override concept can be extended to use of the Bezel button 156 (Fig. 2), connected to the POWERBTN_ input of the power management controller 126 in the PCI-ISA bridge 124 to place the computer either into the Sleep or Soft-Off state.

In one embodiment, whether the PCI-ISA bridge 124 can transition the computer 8 into Sleep state depends upon control bits set in the processor control register in the PCI-ISA bridge 124. The processor control register includes a Sleep enable (SLEEP_EN) bit and a clock control enable (CC_EN) bit, which both are set high to enable Sleep state. If the CC_EN and SLEEP_EN bits are set, then the SMI handler can transition the computer 8 into Sleep state by performing a read of a processor level 3 (PLVL3) register in the PCI-ISA bridge 124. Reading to this register causes the PCI-ISA bridge 124 to generate signals to cause the computer 8 to enter the Sleep state. In response to a read of the PLVL3 register, the power system management controller 126 in the PCI-ISA bridge asserts a signal STPCLK_, which causes the CPU 100 to issue a stop grant bus cycle. When the stop grant bus cycle is terminated, and after a predetermined number of PCI clock cycles on the PCI bus 106, the PCI-ISA bridge asserts its SLP_ signal. Various processor clocks are disabled to enter Sleep state. In addition, the video controller 108 shuts down the VSYNC and HSYNC signals to blank the monitor 6.

It is also possible to enter into other types of intermediate power states, such as the stop grant state, the stop clock state (if a Pentium II CPU is used), or a deep sleep state (if a Pentium II CPU is used). Each of these states corresponds to a unique combination of the CC_EN, SLEEP_EN, and STPCLK_EN bits in the processor control register of the PCI-ISA bridge 124. Thus, if desired, the processor control register can be programmed to enter one of these other states in response to the user pressing the Sleep button 118 for less than the predetermined time period.

Another intermediate power state is the power-on suspend (POS) mode, in which all devices are powered up except for the clock synthesizer in the PCI-ISA bridge 124. The host and PCI clocks are inactive and the PIIX4 chip provides control signals and 32-kHz suspend clock to allow for DRAM refresh and to turn off the clock synthesizer. The only power consumed in the system is due to DRAM refresh and leakage current of the powered up devices.

Alternatively, if the PCI-ISA bridge 124 does not include a clock synthesizer, the host and PCI clocks remain active but the clocks to the internal circuitry of the PCI-ISA bridge are stopped to conserve power. Entry into the POS mode is accomplished using SUS_EN and SUS_TYP bits in a power management control register of the PCI-ISA bridge 124, and is described in further detail below in connection with entering the suspend states.

The computer 8 can be taken out of the Sleep state and restored to full operation either by system hardware or software. The SMI handler, invoked in response to activation of the Sleep button 118 on the monitor 6, is one example of software that can bring the computer back to full operation by clearing the CC_EN bit in the processor control register of the PCI-ISA bridge 124.

If the one-second timer was restarted four times by the SMI handler in response to the user activating the Sleep button 118 on the monitor 6 for more than 4 seconds, the parameter TSLEEP will have counted to the value 4, and the SMI handler transitions to step 520 to place the computer into the Soft-Off mode.

The PIIX4 chip supports the Soft-Off and suspend to RAM (STR) suspend modes.

In the STR mode, power is removed from most of the computer's components except the DRAM and the RTC and certain system power management circuitry in the PIIX4 chip. Of the suspend modes, the Soft-Off is the mode of least power consumption, in which power is maintained only to the RTC and certain of the system power management circuitry in the PIIX4 chip.

The type of suspend mode is enabled by setting the suspend type (SUS_TYP) bits in the power management control register of the PCI-ISA bridge 124 to a particular value. If the SUS_TYP bits are set to 000, then the Soft-Off mode is selected. A value of 001 selects the STR mode, respectively.

To initiate placing the computer 8 into the Soft-Off state at step 520, the SMI handler sets the SUS_EN bit and the appropriate value in the SUS_TYP bits in the power management control register of the PCI-ISA bridge 124. In response, the system power management controller 126 in the PCI-ISA bridge 124 asserts the signal SUSC_ to the inverters 154, which drives the signal SUSC to the power supply 152 to shut down all supply voltages except VCC(RTC) and VCC(SUS).

To enter the intermediate power POS state, the SMI handler would set the SUS_EN bit and write the value 100 into the SUS_TYP bits.

A hardware event that can cause the computer 8 to transition out of the Soft-Off state is activation of the SLEEP button 118 on the monitor 6, which causes the LID signal to be asserted by the inverter 122. In response to the assertion of the LID signal, the PCI-ISA bridge 124 deasserts the signal SUSC_ to allow the power supply 152 to bring all supply voltages to power-on levels. Once the supply voltages are stable and have reached proper power-on voltage levels, the power supply 152 asserts a signal PWROK to the PCI-ISA bridge 124 to indicate that the supply voltages have been powered on. The system reset controller 130 in the PCI-ISA bridge 124 then performs a reset (by asserting reset signals) of all of the components in the computer 8 to reboot the computer.

Other embodiments are also within the scope of the following claims. For example, the order of the steps described for the microcontroller firmware, the BIOS routine, and the SMI handler can be varied and still achieve desirable results. In addition, instead of using the PCI-ISA bridge 124, different controller chips can be used to interact with the BIOS routines and SMI handler to control the power state of the computer 8. Also, a different existing wire in the video cable (such as a VGA cable) can be used to route the sleep indication.

Claims

1. A power management controller for controlling a power state of a computer including a monitor having a power control button, the power management controller comprising:

   means for detecting activation of the power control button; and

   a controller configured to change the power state of the computer in response to activation of the monitor power control button.

2. A computer system, comprising:

   a monitor having a power button; and

   a power management controller according to claim 1.

3. The computer system of claim 2, wherein the power management controller includes a bus device.

4. The computer system of claim 3, wherein the bus device includes a PCI-ISA bridge chip.

5. The computer system of claim 4, wherein the bus device includes a PIIX4 PCI-ISA bridge chip.

6. The computer system of any of claims 2 to 5, wherein the power management controller includes a system management interrupt handler.

7. The computer system of any of claims 2 to 6, wherein the power management controller is coupled to the monitor over a video cable, and wherein activation of the monitor power control button is indicated by a signal transmitted over a wire of the video cable.

8. The computer system of claim 7, wherein the video cable includes a VGA cable.

9. The computer system of claim 7 or claim 8, wherein the monitor includes a microcontroller configured to enable transmission of the activation of the monitor power control button over the video cable.

10. The computer system of claim 8 or claim 9, further comprising:

    a serial bus cable coupling the monitor and the power management controller,

    wherein the microcontroller is further configured to enable transmission of the activation of the monitor power control button over either the video cable or the serial bus cable.

11. The computer system of claim 10, wherein the serial bus cable includes a Universal Serial Bus cable.

12. The computer system of any of claims 2 to 11, wherein the power control button includes a sleep button.

13. The computer system of any of claims 2 to 12,

wherein the computer includes at least two of the following states: a suspend state, an intermediate power state, and an ON state.

14. The computer system of claim 13, wherein the suspend state includes a Soft-Off state.

15. The computer system of any of claims 2 to 14, wherein the power management controller is configured to determine the type of monitor, the power management controller enabling the control of the power state of the computer system only when the monitor is determined to be a power control-type monitor.

16. The computer system of claim 25, wherein the power management controller includes a BIOS routine.

17. The computer system of any of claims 2 to 16, further including a mass storage device accessible by the power management controller.

18. The computer system of claim 13, wherein the power management controller places the computer system into the suspend state if the power control switch is activated continuously for greater than a predetermined time period.

19. The computer system of claim 18, wherein the power management controller places the computer system into the sleep state if the power control switch is activated for less than a predetermined time period.

20. A method of controlling a power state of a computer, the computer being connected to a monitor having a power control button, the method comprising:

receiving activation of the monitor power control button; and
changing the power state of the computer in response to activation of the monitor power control button.

21. The method of claim 20, wherein the computer is connected to the monitor over a video cable, and wherein the receiving step includes receiving an activation signal representing activation of the monitor power control button over a wire of the video cable.

22. The method of claim 21, wherein the video cable includes a VGA cable having a pin 4, and wherein the activation signal is transmitted through pin 4.

23. A method according to any of claims 20 to 22, further comprising:

generating a system management interrupt in response to receipt of the activation signal; and
invoking a system management interrupt handler to change the power state of the computer, and
wherein the computer includes an ON state, an intermediate power state, and a suspend state.

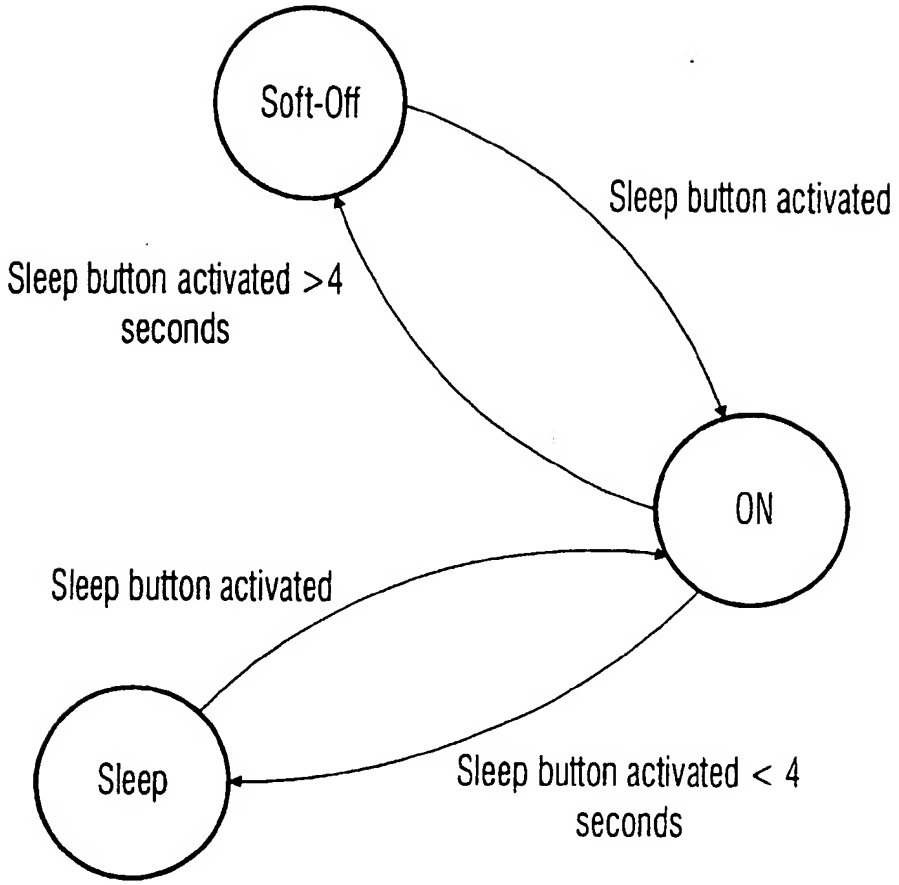
Soft-Off
Sleep button activated
Sleep button activated >4 seconds
ON
Sleep button activated
Sleep
Sleep button activated < 4 seconds

Figure 1

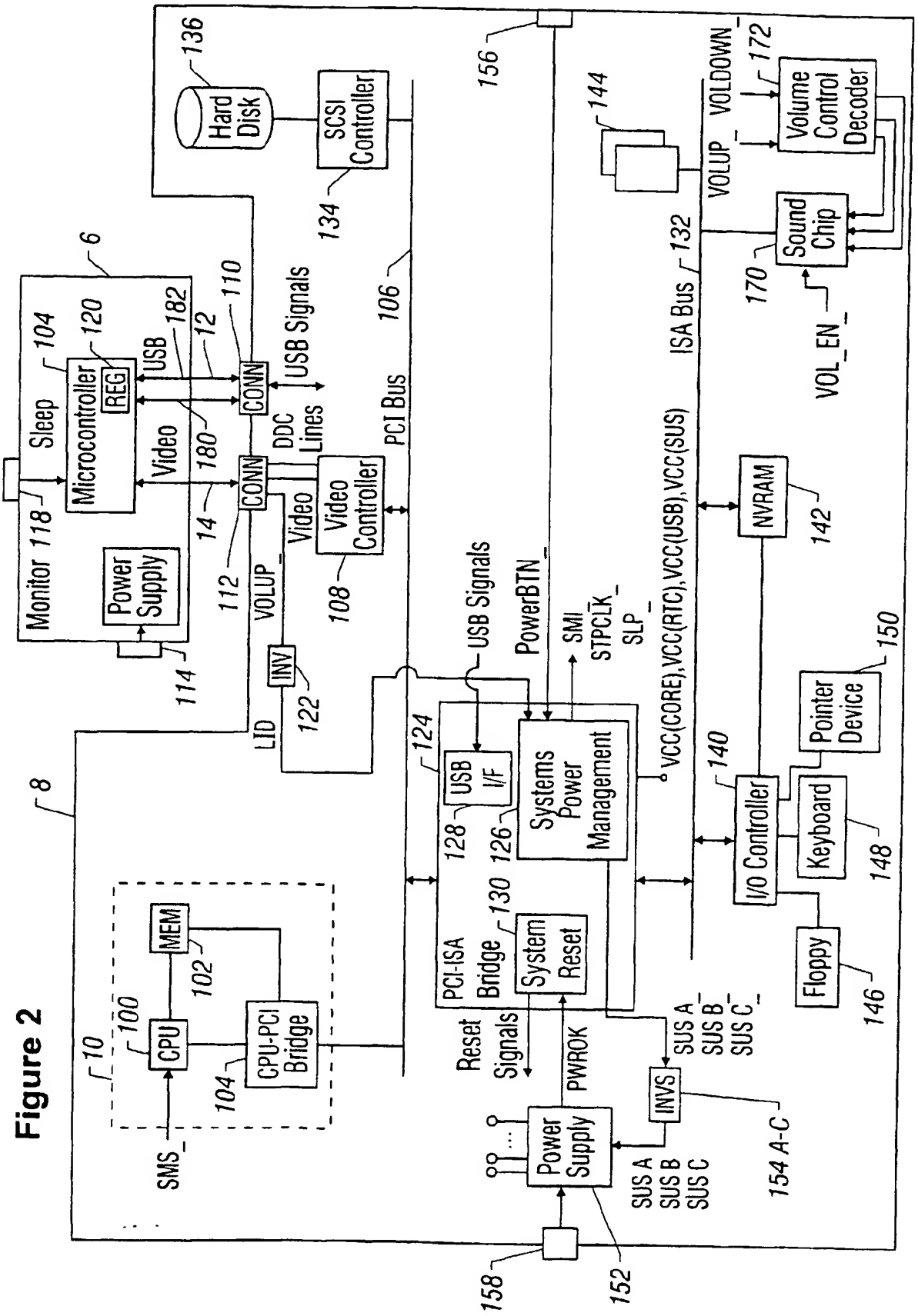
Hard Disk
136
SCSI Controller
134
156
144
VOLUP_
VOLDOWN_
172
Volume Control Decoder
Sound Chip
170
VOL_EN_
ISA Bus
132
6
Sleep
104
Microcontroller
REG
120
USB
182
12
110
CONN
USB Signals
106
PCI Bus
Monitor 118
Power Supply
114
Video
180
14
CONN
DDC Lines
Video
Video Controller
108
112
VOLUP_
INV
122
LID
USB Signals
PowerBTN_
SMI
STPCLK_
SLP_
VCC(CORE),VCC(RTC),VCC(USB),VCC(SUS)
NVRAM
142
8
124
USB I/F
128
126
Systems Power Management
140
Pointer Device
150
I/O Controller
Keyboard
148
Floppy
146
PCI-ISA Bridge
130
System Reset
Reset Signals
PWROK
SUS A
SUS B
SUS C
INVS
154 A-C
10
100
CPU
MEM
102
CPU-PCI Bridge
104
SMS_
Power Supply
SUS A
SUS B
SUS C
158
152

Figure 2

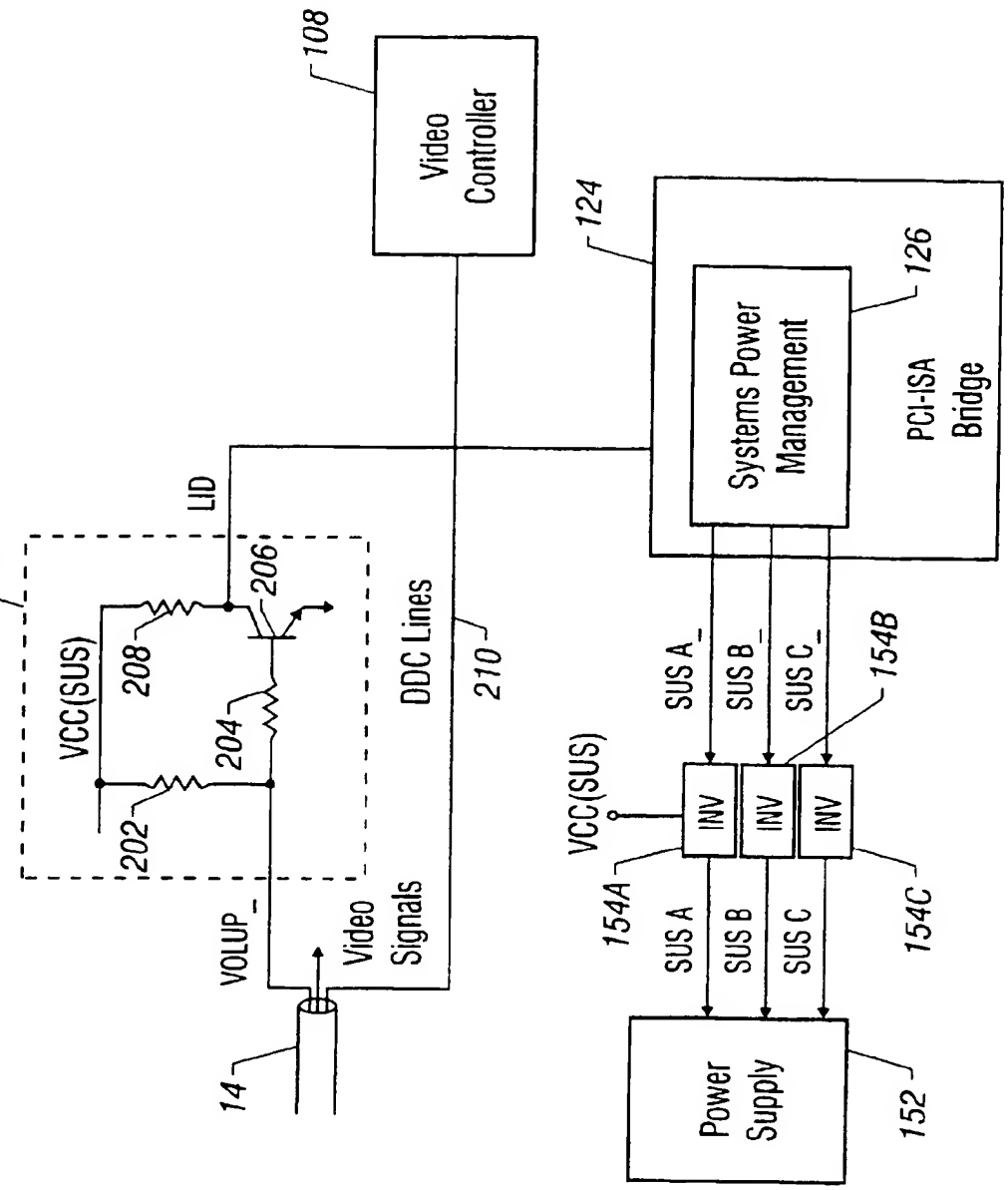

Figure 4

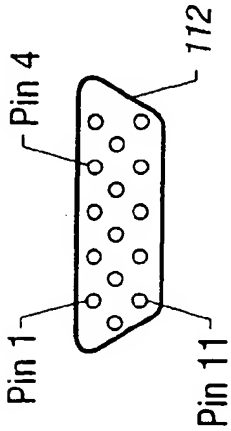

Figure 3

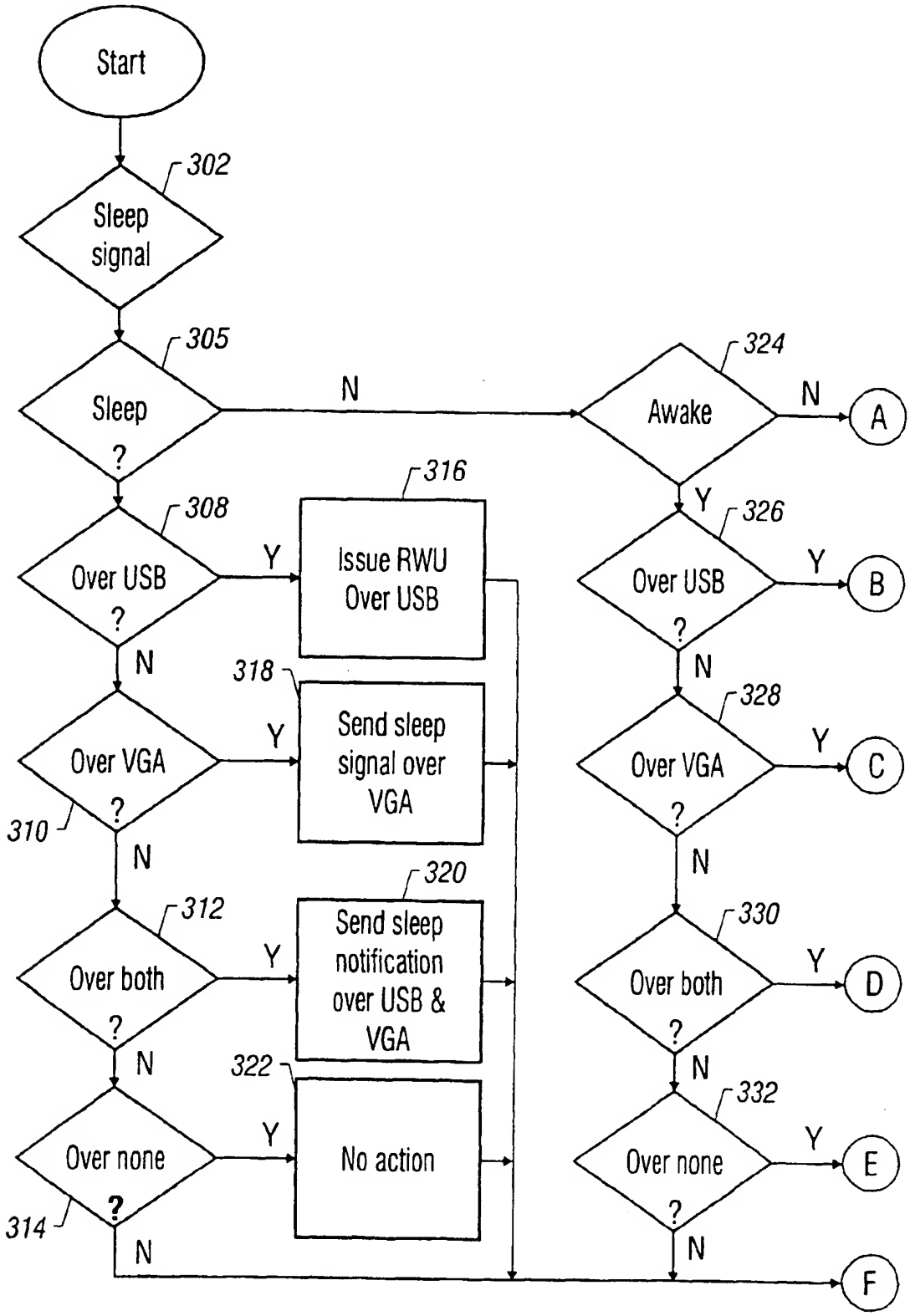
Start
302
Sleep signal
305
Sleep ?
N
324
Awake
N
A
Y
316
308
Over USB ?
Y
Issue RWU Over USB
326
Over USB ?
Y
B
N
318
Send sleep signal over VGA
328
Over VGA ?
Y
C
310
Over VGA ?
N
320
312
Over both ?
Y
Send sleep notification over USB & VGA
330
Over both ?
Y
D
N
322
No action
332
Over none ?
Y
E
314
Over none ?
N
N
F

Figure 5A

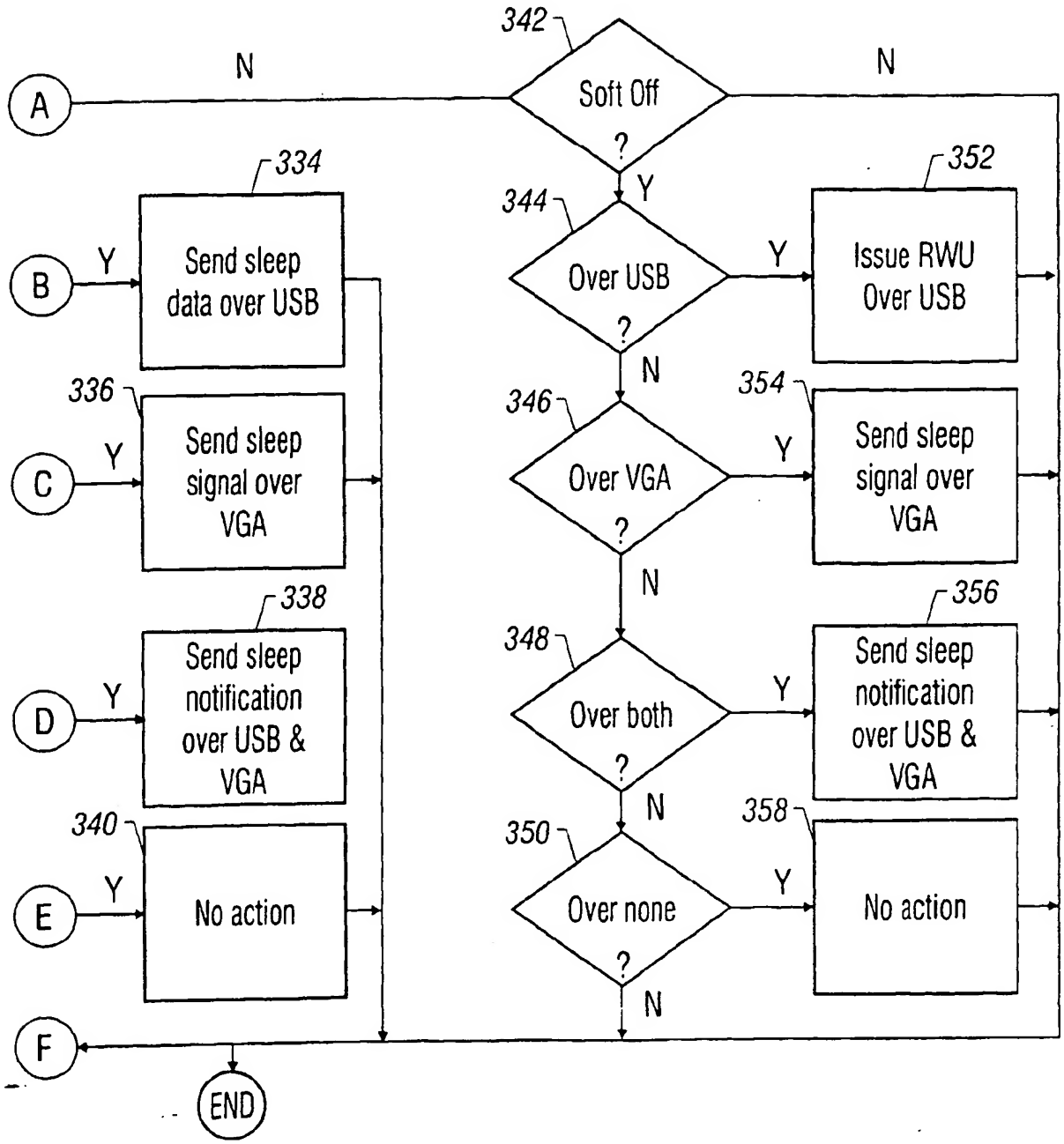
342
Soft Off
?
N
N
Y
A
334
Send sleep data over USB
B
Y
336
Send sleep signal over VGA
C
Y
338
Send sleep notification over USB & VGA
D
Y
340
No action
E
Y
F
END
344
Over USB
?
Y
352
Issue RWU Over USB
N
346
Over VGA
?
Y
354
Send sleep signal over VGA
N
348
Over both
?
Y
356
Send sleep notification over USB & VGA
N
350
Over none
?
Y
358
No action
N

Figure 5B

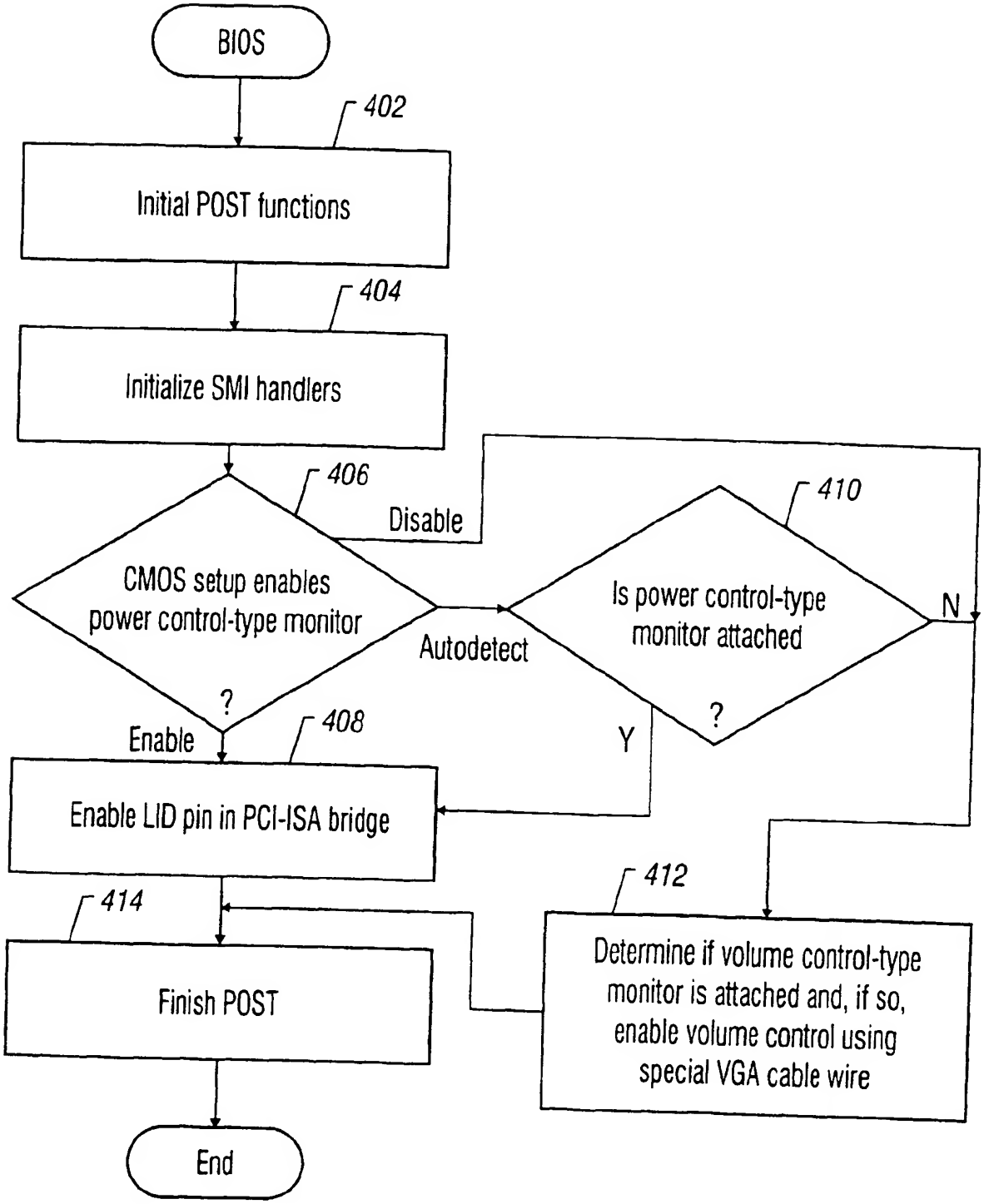
BIOS
402
Initial POST functions
404
Initialize SMI handlers
406
CMOS setup enables power control-type monitor
?
Disable
Autodetect
Enable
408
Enable LID pin in PCI-ISA bridge
410
Is power control-type monitor attached
?
N
Y
412
Determine if volume control-type monitor is attached and, if so, enable volume control using special VGA cable wire
414
Finish POST
End

Figure 6

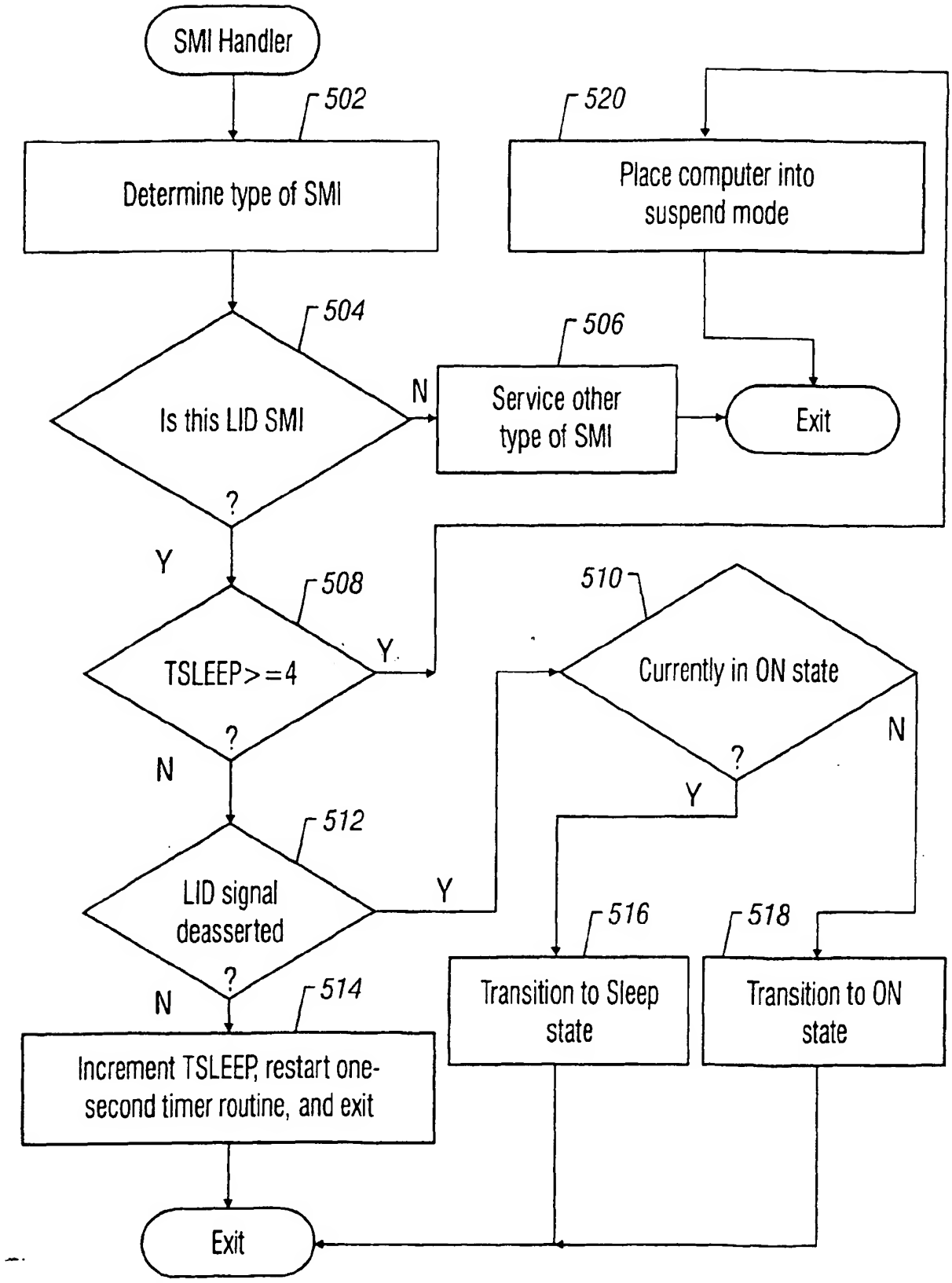
SMI Handler
502
Determine type of SMI
504
Is this LID SMI
?
N
506
Service other type of SMI
Exit
520
Place computer into suspend mode
Y
508
TSLEEP>=4
?
Y
N
510
Currently in ON state
?
Y
N
512
LID signal deasserted
?
Y
N
514
Increment TSLEEP, restart one-second timer routine, and exit
516
Transition to Sleep state
518
Transition to ON state
Exit

Figure 7

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European Patent Office
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(54) Controlling a power state of a computer

(57) Method and apparatus of controlling a power state of a computer, the computer being connected to a monitor having a power control button. The computer is connected to the monitor over a video cable, and activation of the power control button is communicated to the computer over a wire in the video cable. In response to the activation signal, a system management interrupt is generated to invoke an SMI handler to change the power state of the computer. The power states of the computer include an ON state, an intermediate power state (such as Sleep state), and a suspend state (such as Soft-Off state).

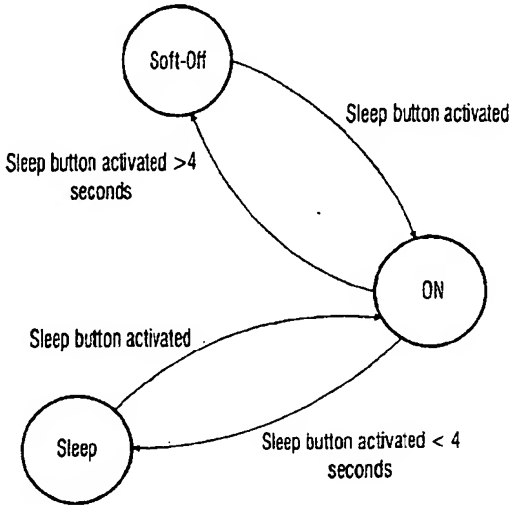

Figure 1

EP 0 889 387 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 30 5147

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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X	WO 94 29783 A (VOBIS MICROCOMPUTER AG ;DAHMEN HEINZ WILLI (DE)) 22 December 1994 (1994-12-22) * page 2, paragraph 2 - page 3, paragraph 1 * * page 4, paragraph 4 * * figures 1,2 *	1-6,13, 17,20,23	
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G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 April 2000	Ciarelli, N

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